1 Introduction

This document describes the highest-level requirements for the NOVA Data Acquisition (DAQ) System Hardware.

2 High Level Requirements

This section describes DAQ System requirements that are necessary to achieve the goals of the NOVA experiment. Note that "timeslice" in this document refers to data from a large (fixed) number of front-end clock periods. A timeslice is typically the longest period of time for which data from the full detector can be conveniently buffered and processed in a single Processor (of order 10 milliseconds).

2.1 Input Rate Requirements

Most of the data produced by the detector is below predetermined thresholds and is suppressed in the front-end electronics. The remaining data volume is estimated at 2.5 X 10^{10} bits per second and must be processed by the DAQ System. This estimate is based on a total of 761,856 front-end channels at an average rate of 400Hz, and allowing 10 data bytes per hit. A factor of 4X in bandwidth capacity is provided to accommodate encoding overheads, variations in occupancy and thresholds, and other readout system inefficiencies. The DAQ System may provide additional data reduction through header consolidation. All data presented to the DAQ System electronics is expected to be in digital form.

- **Input data rate:** The DAQ System must accept a total data rate of at least 1 X 10^{11} bits per second (at least 4 X 10^{6} bits from each front-end module).

2.2 Output Rate Requirements

Two types of data will be collected. Data coincident with the Fermilab neutrino beam spill is always recorded to permanent storage. This data represents a 30usec window in each 2 second machine cycle, or ~0.002% of the total input data rate. Background data (outside of the spill window) is collected by the DAQ, but is only recorded to permanent storage if a Supernova trigger is detected. Some of the output data may be summarized, resulting in a reduction in data size.

- **Output data rate:** The DAQ System must be capable of delivering a data rate of 2 X 10^{6} bits per second from the Processors to the Data Storage system.
- **Reverse datapath:** The DAQ System must be capable of delivering data from the Data Storage system to the Processors, allowing offline use of the Processors when the detector is not operating.

3 DAQ Electronics

The hardware components of the NOVA DAQ System are described in this section. The first elements of the data acquisition system are the Data Concentrators. Front-end electronics requirements are described in a separate document.

3.1 Generic

The following requirements apply to all components of the DAQ Electronics.

- **Control & Status:** The DAQ Electronics must respond to Run Control commands and must provide error and status information to the appropriate error handling/recovery and status monitoring systems.
- **Fault Tolerance:** The DAQ Electronics must continue to operate in the presence of faults, such that only data from the failed component is affected. Error detection must be sufficient to automatically identify and isolate failed components.
- **Synchronization:** At every stage of the readout chain a synchronization mechanism shall be provided that relates data fragments to a specific front-end clock.

3.2 Data Concentrators

The DAQ System will provide a standard component (Data Concentrator) for receipt of digital data from front-end modules. The Data Concentrator will also distribute control, monitoring and timing information as well as configuration information such as thresholds to/from the front-end modules.

- **Number of Front-end Ports:** The Data Concentrator must accept data from as many front-end boards as necessary to effectively utilize the bandwidth of the output data link.
- **Input Link Protocol:** The input link protocol must include error detection and automatic resynchronization on packet boundaries.
- **Processing:** The Data Concentrator must be capable of performing header consolidation and high-level data packet formatting (e.g., Ethernet).
- **Remote Access:** The Data Concentrator must be remotely resetable and reconfigureable under all conditions not involving hardware failure of the module.
- **Timing Distribution:** The Data Concentrator must distribute control and synchronous timing signals to each front-end module.
- **Multiplexing:** The Data Concentrator must assemble the data received from all connected input channels during a period of one timeslice for delivery to a specific Processor.
- **Routing:** The Data Concentrator must be capable of routing data to destination Processors based on a list of active Processors and a predetermined output sequence that can be unique to each Data Concentrator.
- **Data Buffering:** The Data Concentrator must provide a logical buffer (queue) for each destination Processor to a depth of at least two timeslices.
- **Output Packet Size:** To maximize network efficiency, Data Concentrator network interfaces must support the largest packet size allowed by the networking standard ("jumbo" data frames in the case of Gigabit Ethernet). Note: a single Data Concentrator will output approximately 8KB (~one "jumbo" Ethernet frame) per millisecond of operation. A minimum timeslice size of 10 milliseconds is suggested for high network efficiency.

3.3 Data Links and Data Network

- **Data Rate:** The Data Network must be capable of delivering a combined rate of 1×10^{11} bits per second from the Data Concentrators to the Processors.
- **Error Detection and Recovery:** The link protocol must provide error detection and automatic resynchronization on packet boundaries.

- **Data Routing:** The Data Network must be capable of routing data from 1) any Data Concentrator to any Processor, 2) any Processor to Global Data Storage, and 3) Global Data Storage to an external network.
- **Data Buffering:** The timeslice builder in the Processor must provide buffer space for at least two full detector timeslices, so that Processors are not idle due to data transfer latency.
- **Timeslice Assembly:** Data from a given timeslice will be assembled on a single node, i.e., the building of a single timeslice is not distributed between Processors.
- **Packet Size:** All Data Network components must support the largest packet size allowed by the networking standard ("jumbo" data frames in the case of Gigabit Ethernet).

3.4 Processor Farm

- **Processor Memory:** For a system with N Processors, each Processor must be capable of holding the full data output of the detector for a period of at least 20/N seconds. This provides a 20 second data history (distributed across N Processors) for supernova events. As an example, a 250 Processor system would require 80 milliseconds of buffer space in each Processor (~1 GByte).
- **Input Packet Size:** Processor Network Interfaces must support the largest packet size allowed by the networking standard ("jumbo" data frames in the case of Gigabit Ethernet).

3.5 Data Storage

There are two layers of data storage, the local disk drives attached to the processors and a network attached central storage system. The local storage is used to quickly offload processor memory in the case of a supernova trigger. Data can then be sequentially transferred to central (global) storage over a longer period of time.

- **Local Storage:** In the event of a Supernova trigger, local disk drives attached to each Processor must be capable of storing data for that processor's timeslice of the supernova acquisition window. Time to offload the Processor memory to local disk should not exceed 5 seconds.
- **Global Storage Rate:** The global data storage system must be capable of accepting a continuous data rate of 2×10^6 bits per second. This is based on a maximum DAQ bandwidth of 1×10^{11} bits per second, and a maximum spill window of 40usec/2 sec (0.002%).
- **Processing:** The global data storage system must be capable of concatenating data fragments from multiple Processors into a single data file.
- **Capacity:** The global data storage system must provide six months of online disk storage (approximately 5 TBytes) in a removable format. If a reliable 2 Mbps data link exists between the NOVA experiment and Fermilab, this capacity can be reduced to one month.

3.6 Timing and Control System

The Timing system ensures synchronization of all front-end electronics. It is assumed that only the Data Concentrators and associated front-end electronics will require low-level synchronous timing, and that all other components of the DAQ System operate asynchronously. A second level of synchronization exists between the NOVA detector and the Fermilab accelerator complex to identify periods of beam spill.

- **Synchronous Clock:** The Timing System must provide a clock that is frequency and phase synchronous across all outputs, and must distribute this clock to all Data Concentrators and front-end modules.

- **Synchronous Commands:** The Timing system must provide at least one clock synchronous signal for the purpose of aligning commands to specific clock edges, and must distribute this signal to all Data Concentrators and front-end modules.
- **Asynchronous Control Distribution:** The DAQ system must provide bidirectional links for control, download and monitoring of each component in the DAQ and front-end electronics. Data and Control links may be shared if control and data packets are easily identifiable.
- **Beam Spill Synchronization:** The Timing system must receive a time-of-day signal accurate to +/- 1 microsecond (most likely via GPS) for the purpose of framing data acquisition of the neutrino beam spill. The timing system must also receive timely communication of beam spill start time via direct or Internet link to the Fermilab accelerator complex such that spill data is correctly identified and recorded..
- **Free-running Beam Spill Synchronization:** The accuracy of the time-of-day signal must be such that the Timing system can predict the start of beam spill, and continue to correctly record spill data, in the absence of a link to the Fermilab accelerator complex for as long as the beam spills remain periodic.
- **Spill and Timeslice Synchronization:** If feasible, timeslice boundaries should be aligned so that a beam spill is contained within a single timeslice, and timeslices containing beam spill data are uniformly distributed across Processors.

3.7 Firmware

Components of the DAQ will include embedded software in the form of FPGA firmware and microcontroller code. This code will be developed using application specific tools including compilers, debuggers, and diagnostic software.

- **Software Repository:** All firmware (source and object code) must reside in a software repository that will be used to keep track of different versions of the firmware as it is being developed.
- **Version Control:** The version number of the firmware that is used to process data must be managed in such a way that the firmware version that was used can always be identified. During operation, the DAQ system should be able to verify firmware version consistency.
- **Development Tools Archival:** The development software and operating environment necessary to recreate the last implemented version of firmware for each component must be archived. Any unique hardware platforms or keys used in the firmware development process must also be identified and tracked.

3.8 Reliability

- **Burn-in:** The DAQ System hardware must undergo a burn-in process to minimize infant mortality failures in the production system.
- **Low-stress Design:** Circuit board assembly techniques must be employed to minimize component stress that would adversely affect reliability.
- **Fault Tolerance:** A level of fault-tolerance and redundancy must be designed into the architecture so that a noticeable percentage of processing elements must fail before the normal operation of the system is significantly affected.
- **Uptime:** The DAQ System must be ready to run during 95% of beam time (no more than 5% dead time for initialization, startup, etc.)

3.9 Test Features

- **Self-test:** DAQ components must include built-in test structures such that internal functions of the module may be tested with minimal use of external test equipment.
- **Interface Test:** DAQ components must include built-in pattern generation and checking such that the interfaces to upstream and downstream components may be tested with minimal use of external test equipment.

3.10 Maintainability

- **Maintenance:** The DAQ system must be maintainable by module replacement.
- **Modularity:** The cost, size and complexity of individual circuit boards must be minimized, such that replacement of a board can be considered a viable repair option.
- **Programming:** All programmable components must be "in-circuit" reprogrammable. If there is no permanent data link to the component, the programming interface must be accessible without removing the component from the system.

3.11 Module and Link Identification

All electronics modules and links require identification. All module and link information will be stored in a database.

- **Module Identification:** Each electronics module must have a label containing a unique bar code and its alphanumeric equivalent. Any module with a control system connection must also be identifiable by a unique electronic tag, which may be a network address.
- **Link Identification:** Each cable must have a label containing a unique bar code and its alphanumeric equivalent, and must be labeled at both ends.

4 Infrastructure and Integration

4.1 Control Network

The Control Network provides a general-purpose interconnection for all subsystems in the NOVA experiment.

- **Control Network Bandwidth:** The Control Network must provide sufficient bandwidth for efficient database access, download, monitoring, slow control and run control functions.
- **Broadcast:** The Control Network must support a broadcast capability.

4.2 Control Room

- **Accessibility:** The Control Room should be implemented as a "remote" facility even if located in the detector building. All information must be electronically accessible over a standard network.

4.3 Test Stands

To the extent possible, all NOVA electronics will include built-in self-test features. Test stands for these individual components will consist mainly of a small power source and a means of connecting the component to a standard desktop PC. For larger system tests, a test stand that simulates the actual operating environment (full system rack) will be necessary. An attempt will be made to minimize the number of components designed solely for test purposes.

- **Component Test Stands:** A standard development/test system including user modifiable, application-specific software and benchtop power must be provided for testing of individual electronics components.
- **System Test Stands:** A standard rack based development/test system including system level software and power must be provided for testing of multiple components in a system environment.

5 Safety and Computer Security

5.1 Safety

- **Low Voltage, High Current Safety:** For low-voltage (less than 50 volts), high-current (greater than 10 amps) power supplies, the safety requirements for high current power distribution systems must be followed. These are detailed in the Fermilab ES&H Manual, Occupational Safety And Health section on Electrical Safety which can be accessed at

  www-esh.fnal.gov/FESHM/5000/5046.html

  A hazard analysis sheet must be completed and signed by any person who will be working with any low-voltage, high-current system, circuit board, or other electronic device. The internal wiring of a commercially manufactured piece of equipment is exempt as detailed in the FESHM section reference above. The reference provides guidance on load connections, ribbon cables, multiple conductors and mechanical components.
- **Computers:** Safety of people or equipment cannot rely on computers or software.

5.2 Security

- **Standards:** The DAQ and Control System must conform to the Fermilab Computer Security Protection Plan.
- **Isolation:** Network architecture must allow rapid isolation from any external network. The DAQ and Control System must be operable when cut off from the external network.

Dependencies

A. Detector and Front-end Electronics Dependencies

A.1 Front-end to Data Concentrator

- **Data Format:** All data presented to the DAQ Data Concentrators must be in digital form.
- **Protocol:** All data presented to the DAQ Data Concentrators must be grouped and identified by timestamp.

A.2 Detector Data Rates

- **Predicted data rates:** The bandwidth requirements of the DAQ System will be based on the estimates of data rates provided by the detector, with some additional margin. These estimates should be as accurate as possible.

A.3 Detector Timing

The Timing system and Data Concentrators will distribute clock and synchronous command signals to front-end electronics.

- **Synchronization:** The front-end board must support a "test and set" command that synchronizes its timestamp counter to a known value at the next synchronous clock. If the state of the counter at the time of the next synchronous clock would not already match this value, a synchronization error must be reported for that front-end board.

A.4 Slow Control

- **Interface:** Interface to the main NOVA Slow Control system must be through a common slow control system package.

B. Facilities Dependencies

B.1 Installation

There are minimum space and power requirements for the DAQ and control electronics.

- **Power and Cooling Requirements:** The DAQ electronics, including Processors and Data Storage, and some spare capacity will require an estimated 100KW of 120 VAC electrical power and associated heat removal. This estimate is based on the following;

256 Processors @ 250W	64KW
372 Data Concentrators @ 20W	8KW
24 Ethenet Switches @ 70W	2KW
Timing System	<1KW
Data Storage, Control Room, Run	
Control Hosts, Database Servers	10KW

Total	85KW

- **Space requirements:** The Processors and Networking equipment will require 8 racks. The Timing system, Run Control hosts and Database servers will require an additional 1-2 racks. Data Concentrators are assumed to be mounted on the detector.
- **Environmental Requirements:** The DAQ electronics will be designed to operate in a normal commercial temperature and humidity environment.